VERIFICATION OF TRANSLATION

I, the below named translator, hereby declare:

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that I am knowledgeable in the English and Japanese languages and that I believe the following is a true and complete translation into the English language of Japanese Patent Application No. 11 - 052323 filed at the Japanese Patent Office on the 1st day of March, 1999 for Letters Patent, including a true translation of the Official Certificate of the Application.

Signed this 4th day of March, 2005

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[Translation of Priority Certificate]

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[Title of the Invention] Complementary Integrated Circuit And Method Of Manufacturing Same

[Claim]

[Claim 1] A complementary integrated circuit comprising:

an n-channel element having a gate electrode made of a first metallic material selected from a group consisting of zirconium and hafnium; and

a p-channel element having a gate electrode made of a second metallic material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

[Claim 2] A complementary integrated circuit according to claim 1, wherein said second metallic material is rhenium.

[Claim 3] A complementary integrated circuit according to claim 1 or 2, wherein said first metallic material has a work function approximate to the work function of n+ polysilicon, and wherein said second metallic material has a work function approximate to the work function of p+ polysilicon.

[Claim 4] A complementary integrated circuit according to any one of the claims 1-3, wherein in said gate electrode constituting said n-channel element, at least a lower layer of said gate electrode in contact with a gate insulating film is made of said first metallic material, and wherein in said gate electrode constituting said p-channel element, at least a lower layer of said gate electrode in contact with said gate insulating film is made of said second metallic material, and wherein a material having a low resistance is arranged at portions except said lower layers of said gate electrode in said n-channel element and of said gate electrode in said p-channel element.

[Claim 5] A method of manufacturing a complementary integrated circuit, comprising the steps of:

forming an n-channel element forming region and a p-channel element forming region on a semiconductor substrate via a predetermined element isolation region;

forming dummy gate electrodes in said regions at the same time;

separately forming predetermined diffusion regions in respective element formation regions with said dummy gate electrodes used as masks;

forming an insulating layer over the entire surface of said

semiconductor substrate including said dummy gate electrodes;

removing one of said dummy gates in said insulating layer to form a first groove therein to be filled with a gate electrode material composed of a first metallic material; and

removing the other of said dummy gates in said insulating layer to form a second groove therein to be filled with a gate electrode material composed of a second metallic material.

[Claim 6] A method of manufacturing a complementary integrated circuit, comprising the steps of:

forming an n-channel element forming region and a p-channel element forming region on a semiconductor substrate via a predetermined element isolation region;

forming an insulating layer over the entire surface of said semiconductor substrate;

forming a first groove in said insulating layer within one of said regions;

filling said first groove with a gate electrode material composed of a first metallic material;

forming a second groove in said insulating layer within the other of said regions;

filling said second groove with a gate electrode material composed of a second metallic material; and

removing said insulating film to thereafter separately form diffusion regions in said regions on said semiconductor substrate with said gate materials used as masks.

[Claim 7] A method of manufacturing a complementary integrated circuit according to claim 5 or 6, wherein in said step of filling said first groove with a gate electrode material composed of a first metallic material or in said step of filling said second groove with a gate electrode material composed of a second metallic material, said gate electrode material to be filled in comprises said metallic material and an electrically conductive material having an appropriate low resistance which are layered one on top of the other in said grooves.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Pertains]

The present invention relates generally to a complementary integrated circuit and a method of manufacturing the same, and more particularly to a complementary MISFET having a plurality of gate electrodes composed of different materials and its manufacturing method.

[0002]

[Prior Art]

Complementary integrated circuits, especially complementary MISFET integrated circuits have hitherto widely been known. In such conventional complementary MISFET integrated circuits, for example, n-type polysilicon containing diffused phosphorus has been widely used as gate electrodes.

The n-type polysilicon is advantageous in that it has a high resistance to heat and chemicals, that it is easy to introduce a high-concentration impurity, and that it is capable of forming a good interface with the gate insulating film. Use of the n-type polysilicon as the gate electrodes may however result in a p-channel FET having a higher threshold value than a desired value. A technique has thus been used for lowering the threshold value of the p-channel FET by means of counter doping (a technique for the p-channel FET in which the p-type impurity is introduced into the substrate only in the vicinity of the surface thereof).

[0003]

Nevertheless, with miniaturization of the integrated circuits themselves there has been a need to lessen the depth of the counter doping impurity to be introduced into the surface, making it difficult to implement the p-channel FET using the n-type gate.

In order to deal with such a problem, in case the gate length is, for example, 0.25 nm or less, a so-called pn gate configuration is employed in which the n-type polysilicon is used for the n-channel FET, and the p-type polysilicon is used for the p-channel FET.

[0004]

Such a pn gate configuration makes use of gate materials suitable respectively for the n-channel type and p-channel type, it is possible to miniaturize the p-channel FET in particular, as compared with the conventional nn gate configuration which uses only the phosphorus diffused n-type polysilicon.

It is relatively easy in the pn gate configuration to form two different gate materials on the same substrate. That is, n-type and p-type polysilicons can be formed by depositing polysilicon which does not contain impurity on the substrate and then by locally introducing by ion implantation n-type impurity into only the n-channel FET region but p-type impurity into only the p-channel FET region.

[0005]

Referring for example to FIG. 7, particularly to FIG. 7(a), a semiconductor layer is formed on an appropriate substrate 1, and an n-well region 3B and a p-well region 3A are formed by way of a predetermined element isolation region 2. Thereafter, a gate insulating film 7 and a polysilicon film 21 are deposited thereon. Gate electrodes 21 are then formed in the respective well regions 3A and 3B as seen in FIG. 7(b).

[0006]

Afterward, as illustrated in FIG. 7(c), only the p-channel FET region for example is covered with a photo resist 201 so that n-type impurity is ion implanted into only the n-channel FET region. Thereby the gate of the n-channel FET is changed to an n-type gate 21A, and n-type source/drain diffusion layers 5A are formed. Subsequently, as shown in FIG. 7(d), only the n-channel FET region is newly covered with a photo resist 201 and p-type impurity is ion implanted into only the p-channel FET region. Thereby the p-channel FET gate is changed to a p-type gate 21B, and p-type source/drain diffusion layers 5B are formed.

[0007]

[Problems to be Solved by the Invention]

By the way, in a complementary MISFET integrated circuit including a combination of two different types of MISFETs, i.e., n-channel type and p-channel type MISFETs, it would be effective to form respective gate electrodes by using different materials for the n-channel FETs and p-channel FETs, in order to achieve a miniaturization or fining down and a high integration degree of the MISFETs.

[0008]

The reason is that the work functions (electrical potential peculiar to the material) of the gate materials suitable for obtaining good characteristics will be different in the n-channel FET and the p-channel

FET and hence that use of a single material may make it difficult for the n-channel FET and the p-channel FET to offer good characteristics at the same time.

More concretely, when the gate material suitable for either one is used, a threshold value of the other becomes too higher than the desired value. In the event of a relatively large MISFET, this deficiency could be overcome by controlling the threshold value by means of the counter doping method. With progress toward miniaturization, it would however be necessary to extremely lessen the distribution depth of the impurity for controlling the threshold value and to achieve a high impurity concentration. Therefore, it becomes difficult to apply the counter doping method thereto.

[0009]

On the contrary, the pn gate configuration can be a technique for separately using two different gate materials. However, the conventional pn gate configuration may suffer from a problem that it is difficult to sufficiently increase the n-type or p-type impurity concentration in the polysilicon.

More specifically, the impurity is introduced by ion implantation from the top surface of the polysilicon, and thence fed by diffusion to the underside thereof which is in contact with the gate insulating film. It would be limitative to raise the diffusion temperature or extend the diffusion time, since there may take place a phenomenon that the impurity (especially p-type boron) penetrates through the gate insulating film.

[0010]

This may result in a lowered impurity concentration at the underside of the polysilicon. Therefore, upon the operation of the FETs, a depletion layer may be formed at the underside of the polysilicon, with the result that the FET gate insulating film may have an increased effective thickness, leading to a deterioration in the performances of the FETs.

This gate depletion problem becomes severer as the FETs get finer and as the gate insulating films get thinner, and it becomes remarkable especially in case the gate length is approximately 0.1 nm or less.

[0011]

On the other hand, it may be possible to solve the gate depletion problem by using metals as the gate materials. The metals are not only

free from occurrence of the depletion, but also are advantageous in that they often tend to lower the gate resistance.

It would also be effective to use semiconductors to which a high-concentration impurity has been doped simultaneously with the depositions.

[0012]

When the metallic gate materials are used or the semiconductors doped upon the depositions are used, there arises a problem that it is difficult to form two different types of gate electrodes on the same substrate.

That is, it is impossible to use the method in which the gates are separately formed of two different gate materials by means of ion implantation as in the conventional pn gates.

[0013]

In general, with respect to the metallic gate electrodes, it is more difficult to perform etching process as compared with the case of polysilicon.

It is therefore an object of the present invention to overcome the above-mentioned drawbacks of the prior art and to provide means for easily manufacturing a fine and high-performance complementary MISFET integrated circuit using different gate materials for the n-channel FET and p-channel FET and capable of suppressing the problem of gate depletion.

[0014]

Another object of the present invention is to obviate a difficulty in processing metallic materials and to provide means for easily manufacturing the complementary MISFET integrated circuit using different metallic gate materials for the n-channel FET and p-channel FET.

[0015]

[Means to Solve the Problems]

In order to attain the above objects, the present invention employs the following technical configurations.

According to a first aspect of the present invention, there is provided a complementary integrated circuit comprising an n-channel element having a gate electrode made of a first metallic material selected from a group consisting of zirconium and hafnium; and a p-channel element having a gate electrode made of a second metallic material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium,

palladium, rhenium and gold.

According to a second aspect of the present invention there is provided a method of manufacturing a complementary integrated circuit, comprising the steps of forming an n-channel element forming region and a p-channel element forming region on a semiconductor substrate via a predetermined element isolation region; forming dummy gate electrodes in the n-well and p-well regions at the same time; separately forming predetermined diffusion regions in respective element formation regions with the dummy gate electrodes used as masks; forming an insulating layer over the entire surface of the semiconductor substrate including the dummy gate electrodes; removing one of the dummy gates in the insulating layer to form a first groove therein to be filled with a gate electrode material composed of a first metallic material; and removing the other of the dummy gates in the insulating layer to form a second groove therein to be filled with a gate electrode material composed of a second metallic material.

[0016]

[Mode for Carrying out the Invention]

The complementary integrated circuit and the method of manufacturing the same in accordance with the present invention thus employ the above-mentioned basic technical configurations. More specifically, by arranging the complementary MISFET integrated circuit in such a manner as to include the n-channel element having a gate electrode made of a first metallic material and the p-channel element having a gate electrode made of a second metallic material, it is possible to avoid depletion of the gate. In addition, by using the gate materials having work functions suitable respectively for the n-channel element and p-channel element, it becomes possible to implement a fine and high-performance complementary MISFET integrated circuit.

[0017]

Furthermore, according to the present invention, the complementary MISFET integrated circuit using different gate materials for the n-channel FET and p-channel FET is produced by the step of forming a first thin film on the semiconductor substrate, the step of forming a first groove or trench in the first thin film, the step of depositing a first gate electrode material so as to fill up the first groove, the step of leaving the first gate electrode

material in the first groove by abrasion or etch back, the step of forming a second groove or trench in the first thin film, the step of depositing a second gate electrode material so as to fill up the second groove, and the step of leaving the second gate electrode material in the second groove by abrasion or etch back. Thus, by using the way of forming the electrodes by abrasion or etch back after filling the groove with the electrode materials, the second gate electrode can be processed and formed without affecting the previously formed first gate electrode. Therefore, it becomes possible to readily form a plurality of different gate electrodes on the same substrate.

[0018]

Furthermore, since the technique of separately forming the gates of different gate materials by ion implantation is not used, any materials could be selected as the gate materials.

Moreover, since etching is not used to process the gate electrodes, any materials hard to etch could be applied to the gate electrodes, thereby providing a wider selectability of the materials.

[0019]

[Working Example]

The present invention will now be described with reference to FIG. 4 which illustrates by way of a specific example the configuration of a complementary integrated circuit and a method of manufacturing the same in accordance with the present invention.

FIG. 4(p) is a sectional view showing the configuration of the specific example of the complementary integrated circuit according to the present invention. In the diagram the complementary integrated circuit is designated at 20 and comprises an n-channel element 21 having a gate electrode 11 made of a first metallic material selected from a group consisting of zirconium and hafnium, and a p-channel element 22 having a gate electrode 12 made of a second metallic material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

[0020]

More specifically, the complementary integrated circuit 20 of the present invention comprises as shown in FIG. 4(p) a semiconductor layer 3 formed on an appropriate substrate 1, the semiconductor layer 3 including a

p-well region 3A and an n-well region 3B which are formed via a predetermined element isolation region 2.

In the n-channel element 21, the gate electrode 11 of the first metallic material is formed on a part of the surface of the p-well region 3A via a gate insulating film 7A. Also, in the p-well region 3A and on both sides of the gate electrode 11, diffusion layers 4A and 5A containing predetermined n-type impurities are formed.

[0021]

Similarly, in the p-channel element 22, the gate electrode 12 of the second metallic material is formed on a part of the surface of the n-well region 3B via a gate insulting film 7B. Also, in the n-well region 3B and on both sides of the gate electrode 12, diffusion layers 4B and 5B containing predetermined p-type impurities are formed.

The second metallic material for use in the present invention is preferably rhenium.

[0022]

In the present invention the semiconductor substrate could also be made of SOI (silicon on insulator) and in such case the p-well region and the n-well region may not necessarily be formed separately especially for the n-channel element 21 and the p-channel element 22.

It is necessary in the present invention that the first metallic material be one having a work function approximate to the work function of n+ polysilicon and that the second metallic material have a work function approximate to the work function of p+ polysilicon.

[0023]

As used herein, the work function refers to an electrical potential proper to that material.

Although in the above specific example, whole portions of the gate electrodes 11 and 12 are formed of the first and second metallic materials, respectively, the present invention is not limited to such configurations. For instance, the gate electrode 11 constituting the n-channel element 21 may employ a multi-layer structure consisting at least of a lower layer made of the first metallic material and being in contact with the gate insulating film 7A, and an upper layer made of a different conductive material having a low resistivity.

[0024]

In the same manner, the gate electrode 11 making up the p-channel element 22 may employ a multi-layer structure consisting at least of a lower layer made of the second metallic material and being in contact with the gate insulating film 7B, and an upper layer made of a different conductive material having a low resistivity.

[0025]

Aluminum, tungsten, titanium, titanium nitride, etc., have hitherto been used as the metallic gate materials although they were not most suitable for both nMOSFETs and pMOSFETs, because their work functions are substantially intermediate between those of n+ polysilicon and p+ polysilicon.

The inventors have found as a result of devoted investigations that zirconium or hafnium are optimum metallic materials because their work functions are closer to that of n+ polysilicon which is most suitable for nMOSFETs.

[0026]

In addition to their appropriate work functions, such metallic materials have excellent features such as a good chemical stability, a great anticorrosion obtained as a result of formation of a steady oxide layer in the air, and a high resistance to heat.

Since such materials have a disadvantage of high electric resistance, it is preferred that a two-layer or multi-layer gate electrode structure be employed which consists of a lower layer made mainly of the first metallic material and being in contact with the gate insulating film and an upper layer made of a low-resistance metal.

[0027]

In this event, it is preferable that a film thickness of zirconium or hafnium film is approximately 3 nm or more.

The metal forming the upper layer is preferably tungsten having a low resistance and easy to process. Also, depending on the situations, it can be various metal silicides such as titanium silicide and the like which are widely used in the conventional silicon processes.

[0028]

Furthermore, the lower end portion of the upper layer metal is

preferably provided with an adhesion layer formed of titanium nitride, tungsten nitride or the like.

It has further been found that platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium, gold, etc. are most suitable as metallic materials having a work function closer to that of p+ polysilicon which is the optimum material for pMOSFETs. In the present invention, one metallic material selected from the group of metal materials is used.

[0029]

Similar to nMOSFETs, in respect of such metals as well, the gate electrode is preferably of the two-layer or multi-layer structure in which the second metallic material is used for only the portion in contact with the gate insulating film 7B and low-resistance metal is stacked at the upper layer portion thereof.

The present invention will also be effective even in cases where n+ polysilicon is used for nMOSFETs or where p+ polysilicon is used for pMOSFETs as in the prior art.

[0030]

More specifically, use of the manufacturing method in accordance with the present invention will allow the gate materials of the nMOSFETs and pMOSFETs to be separately deposited, so that it is possible to introduce n-type or p-type impurities with a high concentration simultaneously with the deposition, in place of introducing impurities into the polysilicon by ion implantation.

By using such method, it is possible to raise an impurity concentration in the vicinity of the gate insulating film as compared with the conventional method, thereby making it possible to restrain the gate depletion.

[0031]

In such case as well, the multi-layer structure could be employed in order to diminish the resistance of the gate electrode, with the use of n+ polysilicon or p+ polysilicon only in the portions in contact with the gate insulating film.

With reference to FIGs. 1 to 4 detailed description will hereinafter be made on the specific example of the complementary integrated circuit and the method of manufacturing the same in accordance with the present invention.

[0032]

Referring to FIGs. 1 to 4, there are shown along the manufacturing process cross sections of the complementary MISFET integrated circuit 20 which is a specific example of the present invention.

In this specific example the source/drain diffusion layers are formed previous to the formation of the gate electrodes.

The p-well 3A, n-well 3B and element isolation insulating film 2 are formed on the semiconductor substrate 1 in a conventional manner, after which a protection film 101 and a film 102 are deposited in sequence (FIG. 1(a)).

[0033]

Using ordinary photolithography and etching, dummy gates are then formed by leaving the films 101 and 102 only at regions where the gate electrodes are to be formed (FIG. 1(b)).

Only the p-channel element region is then covered with a photo resist 201, so that n-type impurities are ion implanted into the n-channel element region to form a shallow n-type source/drain diffusion layer 4A (FIG. 1(c)).

[0034]

The photo resist is then stripped off and only the n-channel element region is newly covered with a photo resist 201, so that the p-type impurities are ion implanted into the p-channel element region to form a shallow p-type source/drain diffusion layer 4B (FIG. 1(d)).

The photo resist is then stripped off, and side wall insulating films 104 are formed at the sides of the dummy gates by an ordinary technique using CVD and etch back (FIG. 2(e)).

[0035]

The same process steps as those shown in FIGs. 1(c) to 2(e) are then carried out to form deep source/drain diffusion layers 5A and 5B (FIGs. 2(f) to 2(h)).

An insulating film 103 is then deposited on the overall surface of the substrate and is planarized by ordinary abrasion or etch back so as to allow the top of the dummy gates to be exposed (FIGs. 3(i) and 3(j)).

[0036]

Only the p-channel element region is then covered with a photo resist 201, so that only the dummy gate in the n-channel element region is

selectively removed (FIG. 3(k)).

The photo resist is then stripped off, and by oxidation of the substrate or by deposition, a gate insulating film 7A is formed in a groove or trench from which the dummy gate is removed. A gate electrode material 11 for n-channel FET is further deposited thereon so as to fill up the groove (FIG. 3(l)).

[0037]

The gate electrode material 11 is then abraded or etched back until the surface of the insulating film 103 is exposed (FIG. 4(m)).

The process steps shown in FIGs. 3(k) to 4(m) are then iterated to form a gate insulating film 7B for p-channel element and a gate electrode 12 (FIGs. 4(n) to 4(p)).

The MISFET 20 is thereafter completed as the complementary integrated circuit through deposition of interlayer insulating films, formation of connection openings to the source/drain diffusion layers and to the gate electrodes, and formation of wiring.

[0038]

In such a specific example, silicon oxide film, polysilicon and silicon oxide film can be utilized in combination as the protection film 101, the film 102 and the insulating film 103, respectively. By using such layered films, it is possible to remove the dummy gates in FIGs. 3(k) and 4(n), by the selective removal of only the polysilicon 102 through etching which uses chlorine gas for example and then by the removal of the thin silicon oxide film 101 through less damaging etching which uses HF (hydrogen fluoride) for example.

[0039]

The bottom portions of the grooves must be subjected to even less damage since they form channels of the FETs. Provision of the protection film 101 will fulfil such a requirement.

With reference to FIGs. 5 to 6, a detailed description will be made on the configuration of another specific example of the complementary integrated circuit and the method of manufacturing the same in accordance with the present invention.

Referring to FIGs. 5 to 6, there is shown along the manufacturing process cross sections of the complementary MISFET integrated circuit

which is another example of the present invention.

[0040]

In this specific example the source/drain diffusion layers are formed after the formation of the gate electrodes.

That is, the p-well 3A, n-well 3B and element isolation insulating film 2 are formed on the semiconductor substrate 1 in a conventional manner, after which a protection film 111 and a film 112 are deposited in sequence (FIG. 5(a)).

[0041]

The protection film 111 and the film 112 can be for example a silicon nitride film and a silicon oxide film, respectively.

Using ordinary photolithography and etching, a groove is then formed at the location where the gate electrode is to be formed (FIG. 5(b)).

A gate insulating film 7A is then formed in the groove by oxidation of the substrate or by deposition, and a gate electrode material 11 for n-channel FET is deposited thereon so as to fill up the groove (FIG. 5(c)).

[0042]

The gate electrode material 11 is then abraded or etched back until the surface of the insulating film 112 becomes exposed (FIG. 5(d)).

The same process steps as those shown in FIGs. 5(b) to 5(d) are then carried out to form a gate insulating film 7B for p-channel element and a gate electrode material 12 (FIGs. 5(e) to 6(g)).

[0043]

The films 111 and 112 are then subjected to selective etching for removal (FIG. 5(h)).

In case the film 112 is a silicon oxide film, hydrogen fluoride can be used for etching. It is to be noted that if the film 111 is thin, it may remain left.

Afterward, in the same manner as in FIGs. 1(c) to 2(h), ion implantation, side wall formation, etc., are carried out to form source/drain diffusion layers 4A, 5A, 4B and 5B (FIG. 6(i)).

[0044]

The MISFET is thereafter completed through deposition of interlayer insulating films, formation of connection openings to the source/drain diffusion layers and to the gate electrodes, and formation of wiring.

In the manufacturing process of the above-mentioned embodiment, the gate electrode 11 remains buried in the insulating film 103 during the formation of the subsequently formed gate electrode 12. For this reason, the gate electrode 12 forming step will not interfere with the gate electrode 11, thus advantageously enabling the two different gate electrodes to readily and separately be formed on the same substrate.

[0045]

Furthermore, processing of the gate materials 11 and 12 can be effected by abrasion. For this reason, it will be possible even for the materials hard to etch to be processed, thus conveniently providing more choice in the materials used.

The above embodiment is arranged such that the source/drain diffusion layers 4A and 5A are self-aligned with the gate electrode 11 and that the source/drain diffusion layers 4B and 5B are self-aligned with the gate electrode 12. This embodiment is therefore applicable to any fine MISFETs of 0.01 nm or less.

[0046]

Usable as the gate electrode material 11 for n-channel element is a stable metal such as zirconium or hafnium having an appropriate work function. Alternatively, it is possible to use n-type polysilicon doped with, e.g., phosphorus simultaneously with the deposition or polysilicon doped with, e.g., phosphorus by diffusion. Available as the gate electrode material 12 for p-channel element is a stable metal such as rhenium having an appropriate work function. In either case, the gate is restrained from becoming depleted as compared with the conventional pn gate configuration.

[0047]

The above description has been made with illustration of the case where the gate electrodes consist of a single layer. However, the gate electrodes may be formed of a plurality of layered materials for the purpose of, e.g., reducing the resistance. For example, the lower and upper layers can be made respectively of a material for determining the work function and a material having a low resistance. To this end, the gate electrode materials 11 and 12 of FIGs. 1 and 2 may form the layered films.

[0048]

In such a case, the gate electrode materials of the above description refer to materials at portions in contact with the gate insulating films at the lowest ends of the gate electrodes. This is due to the fact that the work function to determine the characteristics of the FETs is determined by the lowermost layer of the gate electrodes. When the gate electrodes are composed of the lamination of a plurality of materials, the n-channel FET and the p-channel FET can include the same gate electrode layers except the lowest ends thereof.

[0049]

In the above case, the FETs have had the source/drain diffusion layers each consisting of a shallow portion and a deep portion. However, the source/drain diffusion layers can be of a so-called single drain structure having a single depth. In such case, the steps corresponding to FIGs. 1(e) to 1(h) can be eliminated.

As is apparent from each of the above-described specific examples, the method of manufacturing the complementary integrated circuit in accordance with the present invention comprises for example the steps of forming an n-well region and a p-well region on a semiconductor substrate via a predetermined element isolation region; forming dummy gate electrodes in the regions at the same time; separately forming predetermined diffusion regions in the respective well regions with the respective dummy gate electrodes used as masks; forming an insulating layer over the entire surface of the semiconductor substrate including the dummy gate electrodes; removing one of the dummy gates in the insulating layer to form a first groove therein to be filled with a gate electrode material composed of a first metallic material; and removing the other of the dummy gates in the insulating layer to form a second groove therein to be filled with a gate electrode material composed of a second metallic material. As is apparent from the other of the above-described specific examples, the method of manufacturing the complementary integrated circuit in accordance with the present invention comprises for example the steps of forming an n-well region and a p-well region on a semiconductor substrate via a predetermined element isolation region; forming an insulating layer over the entire surface of the semiconductor substrate; forming a first groove in the insulating layer within one of the regions;

filling the first groove with a gate electrode material composed of a first metallic material; forming a second groove in the insulating layer within the other of the regions; filling the second groove with a gate electrode material composed of a second metallic material; and removing the insulating film to thereafter separately form diffusion regions in the respective regions on the semiconductor substrate with the respective gate materials used as masks.

[0050]

In the step of filling the first groove with a gate electrode material composed of a first metallic material or in the step of filling the second groove with a gate electrode material composed of a second metallic material, it is preferred in the present invention that the gate electrode material to be filled in comprises the metallic material and an electrically conductive material having an appropriate low resistance which are layered one on top of the other.

[0051]

[Effects of the Invention]

According to the present invention as set forth hereinabove there is provided a complementary MISFET integrated circuit easy to manufacture and capable of achieving both the miniaturization and enhancement of performances, on the basis of basic configurations ensuring that the miniaturization is facilitated by allowing use of different gate electrode materials for the n-channel element and the p-channel element, that the high performances are secured by restraining the gates from becoming depleted, and that the configuration including a plurality of gate materials can easily be manufactured by employing the manufacturing method in which the gates are buried in the grooves.

[0052]

It will be appreciated that the present invention is not limited to the above embodiments and that the embodiments can variously be modified without departing from the scope of the technical ideas of the present invention.

[Brief Description of drawings]

[Fig. 1]

FIG. 1 shows sectional views of a semiconductor device in major steps of the procedure for configuring a specific example of a complementary

integrated circuit in accordance with the present invention;

[Fig. 2]

FIG. 2 shows sectional views of the semiconductor element in major steps of the procedure for configuring the specific example of the complementary integrated circuit in accordance with the present invention;

[Fig. 3]

FIG. 3 shows sectional views of the semiconductor element in major steps of the procedure for configuring the specific example of the complementary integrated circuit in accordance with the present invention;

[Fig. 4]

FIG. 4 shows sectional views of the semiconductor element in major steps of the procedure for configuring the specific example of the complementary integrated circuit in accordance with the present invention;

[Fig. 5]

FIG. 5 shows sectional views of a semiconductor element in major steps of the procedure for configuring another specific example of a complementary integrated circuit in accordance with the present invention;

[Fig. 6]

FIG. 6 shows sectional views of the semiconductor element in major steps of the procedure for configuring the another specific example of the complementary integrated circuit in accordance with the present invention; and

[Fig. 7]

FIG. 7 shows sectional views for explaining an example of the conventional method of manufacturing a complementary integrated circuit.

[Explanations of Letters or Numerals]

1···substrate
2···element isolation region
3···semiconductor layer
3A···p-well region
3B···n-well region
4, 5···diffusion regions
7···gate insulating film
8···sidewall
11···gate electrode made of first metal material

12···gate electrode made of second metal material

20···complementary integrated circuit

21···n-channel element

22···p-channel element

101···lower layer film of dummy gate

102···upper layer film of dummy gate

103···insulating film for forming trench

111···dummy lower layer film for forming trench

112···dummy upper layer film for forming trench

[Document's Name] Abstract

[Abstract]

[Problems to be Solved by the Invention] To provide means for easily manufacturing a minute and high performance complementary MISFET integrated circuit, in which a problem of gate depletion is suppressed by using different gate materials for n-channel FET and p-channel FET.

[Means to solve the Problems] A complementary integrated circuit 20 comprises an n-channel element 21 having a gate electrode 11 made of a first metallic material selected from a group consisting of zirconium and hafnium, and a p-channel element 22 having a gate electrode 12 made of a second metallic material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

[Chosen Drawing] Fig. 4